Amendments to the Claims

1. (Currently Amended) A method for fabricating one or more MOS transistors, the method comprising the steps of:

forming a buffer oxide layer on a semiconductor substrate having an isolation layer;

conducting ion implantations for well formation and field stop formation in an active region of the substrate through the buffer oxide layer;

removing the buffer oxide layer;

forming a sacrificial layer on the semiconductor substrate;

patterning the sacrificial layer to form a trench defining a gate electrode forming region; and

conducting ion implantations for threshold voltage adjustment and punch stop formation in the semiconductor substrate area under the trench.

2. (Currently Amended) A method for fabricating one or more MOS transistors, the method comprising the steps of:

forming a buffer oxide layer on a semiconductor substrate having an isolation layer;

conducting ion implantations for well formation and field stop formation in an active region of the substrate through the buffer oxide layer;

removing the buffer oxide layer;

forming a sacrificial layer ~~of~~ on the semiconductor substrate;

patterning the sacrificial layer to form a trench defining a gate electrode forming region;

conducting ion implantations for threshold voltage adjustment and punch stop formation ~~on~~ in the semiconductor substrate area exposed by the trench;

forming a gate oxide layer on the exposed surface of the substrate ~~under the bottom face of the trench~~;

forming a ~~polysilicon~~ gate electrode layer on the sacrificial layer so as to completely ~~bury~~ fill the trench;

polishing the ~~polysilicon~~ gate electrode layer until the surface of the sacrificial layer is exposed, so as to form a gate electrode;

removing the sacrificial layer;

forming an LDD region in the surface of the substrate at both side portions of the gate electrode;

forming spacers on both side walls of the gate electrode; and

forming ~~the~~ source/drain regions in the surface of the substrate at both side portions of the gate electrode including the spacers.

3. (Currently Amended) The method for fabricating MOS transistors as claimed in claim 1 ~~or 2~~, wherein ion ~~implantations~~ implantation for ~~field~~ punch stop formation is conducted only ~~under~~ in the semiconductor substrate ~~to be gate electrode~~ area under the trench.

4. (Currently Amended) The method for fabricating MOS transistors as claimed in claim 1 ~~or 2~~, wherein the sacrificial layer ~~is composed of~~ comprises a chemical vapor deposition (CVD) oxide layer.

5. (Currently Amended) The method for fabricating MOS transistors as claimed in claim 1 ~~or 2~~, wherein the sacrificial layer ~~is formed as to have~~ has a thickness ranging between ~~500~~500Å and ~~1000~~1000Å.

6. (Currently Amended) The method for fabricating MOS transistors as claimed in claim 1, wherein the patterning of the sacrificial layer ~~is implemented by~~ comprises wet-etching ~~process~~ the sacrificial layer.

7. (Currently Amended) The method for fabricating MOS transistors as claimed in claim 1 ~~or 2~~, wherein ~~ion~~ ions implanted for well formation and field stop formation ~~is~~ comprise boron, phosphorous or Arsenic.

8. (Currently Amended) The method for fabricating MOS transistors as claimed in claim 1 ~~or 2~~, wherein ~~implant~~ ion implantation for field stop formation is ~~made~~ conducted at a sufficient energy to form a barrier ~~barriers~~ below ~~the~~ a source /drain junction.

9. (New) The method as claimed in claim 2, wherein ion implantation for punch stop formation is conducted only in the semiconductor substrate area exposed by the trench.

10. (New) The method as claimed in claim 2, wherein the sacrificial layer comprises an oxide layer.

11. (New) The method as claimed in claim 2, wherein the sacrificial layer comprises a chemical vapor deposition (CVD) oxide layer.

12. (New) The method as claimed in claim 2, wherein the sacrificial layer has a thickness ranging between 500Å and 1000Å.

13. (New) The method as claimed in claim 2, wherein the patterning of the sacrificial layer comprises wet-etching the sacrificial layer.

14. (New) The method as claimed in claim 2, wherein ions implanted for well formation and field stop formation comprise boron, phosphorous or Arsenic.

15. (New) The method as claimed in claim 2, wherein ion implantation for field stop formation is conducted at a sufficient energy to form a barrier below a source/drain junction.

16. (New) The method as claimed in claim 2, wherein said gate electrode layer comprises polysilicon.

17. (New) The method as claimed in claim 1, wherein the sacrificial layer comprises an oxide layer.

18. (New) The method as claimed in claim 1, wherein the sacrificial layer consists essentially of an oxide layer.

19. (New) The method as claimed in claim 18, wherein the sacrificial layer has a thickness ranging between 500Å and 1000Å.

20. (New) A method for fabricating a MOS transistor, comprising the steps of:

conducting ion implantations for threshold voltage adjustment and punch stop formation in an exposed semiconductor substrate area, said semiconductor substrate having an isolation layer therein and a patterned sacrificial oxide layer thereon, the patterned sacrificial oxide layer having a trench therein (i) defining a gate electrode forming region and (ii) exposing said exposed semiconductor substrate area;

forming a gate electrode in the trench;

removing the patterned sacrificial oxide layer;

forming an LDD region in the substrate at side portions of the gate electrode;

forming spacers on side walls of the gate electrode; and

forming source/drain regions in areas of the substrate not covered by the gate electrode and the spacers.

Amendments to the Figures

Figures 1A-1C have been amended by adding the label "(PRIOR ART)" below each Figure, as required by the Examiner. Replacement Sheets (as required by 37 C.F.R. 1.121(d)) are attached to this Amendment.